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a	AG8	5,129,067	07/1992	Johnson		<u> </u>		
2	AH8	5,345,569	09/1994	Tran				
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9	-AJ8	6,256,720	07/2001	Nguyen et al.				
4	AK8	5,287,467	02/1994	Blaner et al.				
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.	2105	AB9	5,197,1	36	03/1993	Kimura et al.	-		
		AC9	5,179,5	30	01/1993	Genusov et al.			<u> </u>
	() 2 10 2004	AD9	5,317,7	20	05/1994	Stamm et al.			
4	S MADELANT	AE9	6,647,4	85	11/2003	Nguyen et al.			
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Page 1 of 2 TTY. DOCKET NO. API 19015.C15 (1397.028000F) 10/0 FIRST NAMED INVENTOR: NGUYEN et al. APPLICATION NO. 10/660,671 **FORM PTO-1449** Seventh Supplemental INFORMATION DISCLOSURE STANDED FILING DATE **ART UNIT** September 12, 2003 2183 **U.S. PATENT DOCUMENTS** DOCUMENT **EXAMINER** INITIAL NUMBER DATE NAME CLASS SUB-CLASS **FILING DATE** AA9 AB9 AC9 AD9 AE9 AF9 5,167,035 11/1992 Mann et al. AG9 2003-0056086-3/20/2003 Nguyen et al. AH9 2003-0079113-4/24/2003 Nguyen et al. AI9 2003-0070060-4/10/2003 Nguyen et al. A1 AJ9 2003-0056087-3/20/2003 Nguyen et al. AK9 2004-0093483-5/13/2004 Nguyen et al. Α1 FOREIGN PATENT DOCUMENTS **EXAMINER** INITIAL **DOCUMENT** DATE COUNTRY **CLASS** SUB-CLASS **TRANSLATION** NUMBER Yes AL8 No Yes AM8 No Yes AN8 No Yes **80A** No Yes AΡ No OTHER (Including Author, Title, Date, Pertinent Pages, etc.) AR <u>33</u> AS <u>33</u> ΑT <u>33</u> **EXAMINER** DATE CONSIDERED EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant. 363941_1.DOC GF Rev. 12/03/03

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W	AA10	2004-0093485 A1	3/2004	Nguyen et al.			
w	AB10	2004-0093482 A1	- 05/13/2004	Nguyen et al.			
6/	AC10	6,256,720	07/03/2001	Nguyen et al.			
9	AD10	6,272,619	08/07/2001	Nguyen et al.			
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ATTY. DOCKET NO. APPLICATION NO. SP015.C15 To Be Assigned **FORM PTO-1449** APPLICANT Nguyen et al. INFORMATION DISCLOSURE STATEMENT GROUP FILING DATE Herewith To be assigned U.S. PATENT DOCUMENTS EXAMINER DOCUMENT CLASS DATE NAME SUB-FILING DATE INITIAL NUMBER CLASS AA1 3,346,851 10/1967 Thornton et al. /\ AB1 3,718,912 02/1973 Hasbrouck et al. n 11/1973 AC1 3,771,138 Celtruda et al. AD1 3,789,365 01/1974 Jen et al. 07/1977 AE1 4,034,349 Monaco et al. z_{γ} AF1 4,200,927 04/1980 Hughes et al. AG1 4,228,495 10/1980 Bernhard et al. Fairchild et al. AH1 4,296,470 10/1981 \overline{A} AI1 4,315,314 02/1982 Russo AJ1 Kawakami 4,410,939 10/1983 AK1 Puhl 4,434,461 02/1984 FOREIGN PATENT DOCUMENTS EXAMINER DOCUMENT DATE COUNTRY INITIAL CLASS SUB-TRANSLATION NUMBER CLASS 0 479 390 A2 08/1992 Yes AL1 No 0 426 393 08/1991 Yes No 0 419 105 A2 10/1990 ΕP Yes AN1 No 12/1990 EP 0 402 856 Yes AO1 No 0 377 991 A3 12/1989 Yes AP1 No OTHER (Including Author, Title, Date, Pertinent Pages, etc.) AR 8-Bit Embedded controller Handbook, Intel, 1989, pp. 1-1- 1-19 and 3-1 -3-37. 1 Acosta, Raymond D. et al., "An Instruction Issuing Approach to Enhancing AS Performance in Multiple Functional Unit Processors," IEEE Transactions on Computers, Vol. C-35, No. 9, September 1986, pp. 815-828. Agerwala et al., "High Performance Reduced Instruction Set Processors," IBM ΑT 1 Research Division, March 31, 1987, pp. 1-61. DATE CONSTREED EXAMINER EXAMINER: Initial if reference considered, whether or not citation is in conformance with MDEP 609. line through citation if not in conformance and not considered. Include copy of this form with next Draw communication to Applicant.

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~	AA2	4,45	9,657	07/1984	Murao	↓			
W	AB2	4,47	6,525	10/1984	Ishii	1	·		
1	AC2	4,62	6,989	12/1986	Torii				
h	AD2	4,67	5,806	06/1987	Uchida	1			
6	AE2	4,71	4,994	12/1987	Oklobdzija et al.	↓			
	AF2	4,72	2,049	01/1988	Lahti				
a	AG2	4,75	2,873	06/1988	Shonai et al.	\perp			
1	AH2	4,75	8,948	07/1988	May et al.				
	AI2	4,76	6,566	08/1988	Chuang				
	AJ2	4,80	7,115	02/1989	Torng				
~	AK2	4,85	8,105	08/1989	Kuriyama et al.				
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6	AL2	+	2 751 A2	11/1989	EP				Yes No
h	AM2	0 36	8 332 A2	05/1990	EP				Yes OM
W	AN2	0 35	4 585 A2	02/1990	EP				Yes No
2	A02	0 17	1 595 A2	02/1986	EP				Yes No
	AP2	0 13	6 179 A2	09/1984	EP				Yes No
	1		THER (Inc.	luding Author,	Title, Date, Pertinent Page	ges,	etc.)		
W	AR	2		and Nicolau, *," pp. 221-23	A., "Perfect Pipelining: A 35.	New	Loop	Paralleliz	zation
	AS	Andrews, Distinctions Blur Between DSP Solutions, Computer Design, Vol. 28, No. 9, May 1, 1989, Littleton, Mass., pp. 86-99.							
	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," Computer, Vol. 14, September 1981, pp. 18-27.								
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\[\sqrt{\sq}}}}}}}\sqrt{\sq}}}}}}}}}\sqit{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sq}}}}}}}}\sqrt{\sqrt{\sqrt{\sq}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}	AB4		9,067	07/1992	Johnson				
ω	AC4		4,561	07/1992	Liptay				
11/	AD4	5,15	5,843	10/1992	Stamm et al.				
N	AE4	5,18	7,796	02/1993	Wang et al.				
a	AF4	5,22	6,126	07/1993	McFarland et al.				
N	AG4	5,22	6,170	07/1993	Rubinfeld				
N	AH4	5,23	0,068	07/1993	Van Dyke et al.				
~	AI4	5,35	5,460	10/1994	Eickenmeyer et al.				
N	AJ4	5,44	2,757	08/1995	McFarland et al.				
0/	AK4	5,46	1,715	10/1995	Matsuo et al.				
				FOREIG	N PATENT DOCUMENTS				
EXAMINER INITIAL		DOCU	MENT SER	DATE	COUNTRY	CLA	SS	SUB- CLASS	TRANSLATION
W	AL4	3-14	7134	06/1991	JP				Yes No
W	AM4	2-22	736	01/1990	JP				Yes No
0	AN4	2-87	229	03/1990	JP				Yes No
0/	A04	3-35	322	02/1991	JP				Yes No
6	AP4	64-3	16366	02/1989	JP				Yes No
			THER (Inc.	luding Author,	Title, Date, Pertinent Pag	es,	etc.)		
~	AR	4.	Gross et Workshop	al., "Optimizi on Microprogra	ng Delayed Branches," Proce nmming, October 5-7, 1982, p	edin	gs of 14-120	the 5 th Ar	nnua l
1	AS	4			r, R., "An IBM Second Genera 889, pp. 134–137.	tion	RISC	Processor	-
1	Bakoglu et al., "IBM Second-Generation RISC Machine Organization," 1990, IEEE, pp. 173-178.							990, IEEE,	
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6	AA5		7,156	01/1996	Popescu et al.			
	AB5		8,729	01/1996	Vesegna et al.			
91	AC5		9,911	07/1996	Nguyen et al.			
1	AD5		1,776	10/1996	Popescu et al.			
01	AE5		4,927	11/1996	Scantlin			
12	AF5	5,59	2,636	01/1997	Popescu et al.			
2	AG5		5,837	04/1997	Popescu et al.			
A	AH5	1	7,983	05/1997	Popescu et al.			
1	AI5		1,125	07/1997	Witt et al.			
\sim	AJ5	5,68	9,720	11/1997	Nguyen et al.			
	AK5	5,70	8,841	01/1998	Popescu et al.			
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1	AL5	2-13		05/1990	Japan			Yes No
	AM5							Yes No
	AN5							Yes No
	A05							Yes No
	AP5							Yes No
			THER (Inc.)	luding Author,	Title, Date, Pertinent Pa	ges, etc.)		
	AR	<u>5</u>		et al., "A 80 E, pp. 15.2.1-) Mflops 64-bit Microproces -15.2.4.	ssor for Pa	arallel Co	omputer,"
4	AS	51	Hennessy et al., Computer Architecture: A Quantitative Approach, Morgan Kaufman Publishers, Inc., 1990 (in its entirety).					
H	Horst, R.W. et al., "Multiple Instruction Issue in the NonStop Cyclone Processor," IEEE, 1990, pp. 216-226.							
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	AA6	5,76	8,575	06/1998	McFarland et al.	<u> </u>			
<u> </u>	AB6	5,77	8,210	07/1998	Henstrom et al.	ــــــــــــــــــــــــــــــــــــــ			
2	AC6	5,79	7,025	08/1998	Popescu et al.	╙			
	AD6	5,83	2,205	11/1998	Kelly et al.	↓			
h	AE6	5,83	2,293	11/1998	Popescu et al.	1_			
	AF6	5,96	1,629	10/1999	Nguyen et al.	ļ			
0	AG6	6,03	8,654	03/2000	Nguyen et al.				
\sim	АН6	6,09	2,181	07/2000	Nguyen et al.	1			
\sim	AI6	6,10	1,594	08/2000	Nguyen et al.				
\sim	AJ6	6,12	8,723	10/2000	Nguyen et al.	<u> </u>			
	AK6	5,23	3,694	08/1993	Hotta et al.	1			
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	AN6								Yes No
	A06								Yes No
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9	AR	<u>6</u>		inctionality,"	gh Performance Restricted D Proceedings from ISCA-13,				
	AS	<u>6</u>	Hwu et al., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," IEEE Trans. On Computers, Vol. C-36, NO. 12, December 1987, pp. 1496-1514.						
	Hwu et al., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," Proceedings of the 15 th Annual Symposium on Computer Architecture, June 1988, pp. 45-53.						ith a Computer		
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\mathcal{U}	AR	2	IBM Journa	al of Research	and Development, Vol.	34, No.	1, Ja	nuary 199	0, pp. 1-70.
	AS	2	Succeeding	M Technical Disclosure Bulletin, Overlap of Store Multiple Operation With acceeding Operations through Second Set of General Purpose Registers, Voll 28, b. 6, November 1989, New York, NY, pp. 2727-2728.					on With s, Voll 28,
6	***	7	Jelemensky Application	ons, Electro C	omputer Features Advance Conference Record, Vol.	d Hardw 14, Apr	are Fo	or Real-Ti	me Control s Angeles,

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<i>M</i>	AR	8		William M., Su	uper-Scalar Processor Desig		tation),	copyright
	AS	Johnson, William M., Super-Scalar Processor Design, Prentice-Hall, Inc., 1991 (in its entirety).						
	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," IEEE, 1989, pp. 229-232.							
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N	AR	બ	Parallelia	sm and Its Eff	uniform Distribution of Insteet on Performance," IEEE '089, pp. 1645-1658.	ruction-L Transactio	evel and M ns on Comp	Machine outers, Vol.	
	AS	9)	Superpipe: Architect	Jouppi et al., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," Proceedings of the 3 rd International Conference on Architectural Support for Programming Languages and Operating Systems, April 1989, pp. 272-282.					
\mathcal{O}	AT	ગ	Keller, R 1975, pp.		ead Processors," Computing	Surveys, V	ol. 7 No	. 4, December	
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	AR	<u>10</u>	Lam, M.S.,	"Instruction	Scheduling For Superscalar 990, pp. 173-201.			nu. Rev.
	AS	<u>10</u>	Lee, Ruby	B., "Precisio	n Architecture," COMPUTER,	January	1989, pp. 7	8-91.
	M	10	Melear, C. 9, No. 2,	, Motorola, I April 1989, L	nc., The Design of the 8800 os Alamitos, CA, pp. 26-38.			MICRO, Vol.
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9	AR	11	Murakami,	K. et al., "S	IMP (Single Instruction Str gh-Speed Single-Processor A	eam/Mult	iple Instru	action 1989, pp.
	AS	11	Odnert, D. et al., "Architecture and Compiler Enhancements for PA-RISC Workstations," Proceedings from IEEE Compcon, February 25-March 1, 1991, San Francisco, CA, pp. 214-218.					
	Patent Abstracts of Japan, Vol. 010, No. 089, April 1986, & JP. A, 60 225 943 (Hitachi Seisakusho K K) November 11, 1985.							
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	AN12			<u> </u>					Yes
	A012								Yes
	AP12	.1		<u> </u>			1		No
	AR	12	Patt et al	l., "Critical	Issues Regarding HPS, occeedings of the 18 th A	A High Per	forma	nce n Microp	rogramming,
	AS	12	Patt et al., "HPS, A New Microarchitecture: Rationale and Introduction," Proceedings of the 18 th Annual Workshop on Microprogramming, December 1985, pp. 103-108.						
M	AT	Pleszkun et al., "The Performance Potential of Multiple Functional Unit Processors," Proceedings of the 15 th Annual Symposium on Computer Architecture, June 1988, pp. 37-44.							
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1	AR 1	<u>13</u>	Pleszkun	et al "WISO:	A Restartable Architectu Symposium on Computer Arch	re Using Qu	ieues," Pro June 1987,	oceedings of pp. 290-299.	
	AS	13		t al., The Met ts entirety).	aflow Architecture, Metaf	low Technol	logies, In	c., June	
	ATT	<u>13</u>	S. McGead IEEE, 199	S. McGeady, "The 1960A Superscalar Implementation of the 80960 Architecture,"					
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	AL14							Yes No	
	AM14							Yes No	
	AN14							Yes No	
-	A014							Yes No	
	AP14							Yes No	
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1	AR	14	Smith et Transacti	al., Implement ons on Comput	tation Precise Interrupts ers, Vol. 37, No. 5, May 1	in Pipel 988, Nev	lined Process W York, NY, p	ors, IEEE . 562, 573.	
	AS	14	Proceedin	al., "Implemed gs of the 12^{th} , pp. 36-44.	ntation of Precise Interru Annual International Symp	epts in 1 posium o	Pipelined Pro n Computer Ar	cess," chitecture,	
Á	AT	14	Internati	mith et al., "Limits on Multiple Instruction Issue," Proceedings of the 3 rd international Conference on Architectural Support for Programming Languages and perating Systems, April 1989, pp. 290-302.					
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1	AR	<u>15</u>	Smith, M.: Processor	D. et al., "Bo ," IEEE, 1990,	osting Beyond Static S pp. 344-354.	chedulin	ng in a	Superscal	lar
D	AS	<u>15</u>	Performan	ohi, Gurindar S. and Sriram Vajapeyam, "Instruction Issue Logic for High- erformance, Interruptable Pipelined Processors," Conference Proceedings of the 4 th Annual International Symposium on Computer Architecture, June 2-5, 1987, pp. 7-34.					
	AT	15	Thornton, Corporati	Thornton, J.E., Design of a Computer: The Control Data 6600, Control Data Corporation, 1970, pp. 58-140.					
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9	AR	<u>16</u>	Tjaden <i>e</i> t	al., "Detecti	lon and Parallel I	Execution of :	Independ	dent Insti pp. 889-89	nuctions," 95.		
	AS	<u>16</u>	Tjaden et Trans. On	al., "Represe Computers, Vo	entation of Concur ol. C-22, No. 8, A	rrency with O August 1973,	rdering pp. 752	Matrices, -761.	," IEEE		
	AT /	16		epresentation tion), 1972, p	and Detection of	Concurrency	Using O	rdering Ma	atrices,		
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	AS	<u>17</u>	Purpose Co	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," Proceedings of the 19 th Annual Hawaii International Conference on System Sciences, 1986, pp. 41-50.					
M	pr ⁽ T)	17	Wedig, R.	G., Detection (Dissertation)	of Concurrency in D , June 1982, pp. 1-	179.			Instruction
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1	AR	18	Weiss, R.		ation RISC Processors, On	Special Rep	ort, Marc	ch 30, 1992,
U	AS	Weiss et al., "Instruction Issue Logic in Pipelined Supercomputers," Reprinted from IEEE Trans. On Computers, Vol. C-33, No. 11, November 1984, pp. 1013-1022.						
	AT	18	English L	anguage Trans	slation of Japanese Patent	Appl. No. 6	51-95447,	published May
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	AL19							Yes No
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	AR	<u>19</u>	English L November	anguage Trans 14, 1990, 20	lation of Japanese Pater pages.	nt Appl. No	. 2-278337,	published
	AS	<u>19</u>	English Language Translation of Japanese Patent Appl. No. 3-137729, published June 12, 1991, 7 pages.					
M	AT	19	English I June 24,	anguage Trans	lation of Japanese Pate s.	nt Appl. No	. 3-147134,	published
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	AR	20	Kuga Morio based on t Architectu	o et al., "Per the SIMP (Sing	formance Evaluation o le Instruction Stream ciplinary Graduate Sc	of the Superscal	uction Pi	peline)		
	AS	20	English Language Translation, Kuga Morio et al., "Performance Evaluation of the Superscalar Processor "SIMP" based on the SIMP (Single Instruction Stream/Multiple Instruction Pipeline) Architecture, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, 1990, pp. 337-344, (Document AR20).							
i D	Kuga Morihiro et al., "Low-Level Parallel Processing Algorithm for the SIMP Processor Prototype," Department of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University Vol. 30, No. 12, Dec. 1989, pp. 1603-1611.									
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(1)	AR	21	Processing Systems,	g Algorithm fo Interdisciplin	ation, Kuga Morihi or the SIMP Process mary Graduate Schoo o. 12, Dec. 1989, p	or Prototyp l of Engine	e," Dep	artment o ciences,	f Information Kyushu
	AS	<u>21</u>	US Application 09/336,589, Senter Cheryl et al., June 21, 1999.						
W	AT	21	Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," Proceedings of the 2 nd International Conference on Architectural Support for Programming Languages and Operating Systems, October 5-8, 1987, California.						ort for
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Page 22 of 28 ATTY. DOCKET NO. APPLICATION NO. SP015.C15 To Be Assigned FORM PTO-1449 APPLICANT Nguyen et al. INFORMATION DISCLOSURE STATEMENT FILING DATE GROUP To be assigned Herewith U.S. PATENT DOCUMENTS EXAMINER CLASS INITIAL DOCUMENT DATE NAME SUB-FILING DATE NUMBER CLASS AA22 AB22 AC22 AD22 AE22 AF22 AG22 AH22 AI22 AJ22 AK22 FOREIGN PATENT DOCUMENTS EXAMINER INITIAL DOCUMENT DATE COUNTRY CLASS SUB-TRANSLATION NUMBER CLASS Yes AL22 No Yes AM22 No Yes AN22 No Yes A022 No AP22 OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Notification of Reason for Refusal for Japanese Patent Application No. 2000-AR 22 145123, mailed June 26, 2002, 2 pages. Notification of Reason for Refusal for Japanese Patent Application No. 2000-AS <u>22</u> 145124, mailed June 26, 2002, 2 pages. Notification of Reason for Refusal for Japanese Patent Application No. 2000-22 145125, mailed June 26, 2002, 2 pages. CONSTDERED EXAMINER

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INFORMATION DISCLOSURE STATEMENT

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	AP27	<u> </u>						Yes No			
			OTHER (Incl	uding Author,	Title, Date, Pertinent Pag	es, etc.)					
1	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) English-language translation, Kuga Morihiro et al., "Low-Level Parallel Processing Algorithms for the "Shinpu" Processor Based on the SIMP (Single Instruction Stream / Multiple Instruction Pipelining) Method, Department of Information System, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, December 1989, pages 1603-1624.										
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